EXPRESS MAIL NO.EL615486435US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicant	:	Robert Louis Hodges
Title	:	SELF-ALIGNED GATE AND METHOD
Docket No.	:	850063.542C1
Date	:	December 7, 2000

Prior Application:

Examiner	:	M. Prenty
Art Unit	:	2822
Application No.:		09/170,957

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents:

Please amend the above-identified application as follows:

In the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 09/170,957, filed October 13, 1998. --

In the Claims:

Please cancel claims 1-10, 12, 13 and 21-42.

Please add the following new claims 43-45.

-- 43. A method of forming a feature having a selected dimension comprising:

forming a first layer having a first thickness on a semiconductor substrate;

forming a second layer over said first layer, said second layer having a second thickness thicker than said first layer and being etchable by a different etch chemistry than said first layer;

forming a recess, having vertical sidewalls separated by a width greater than said selected dimensions, said recess extending through said second layer and not through said first layer;

forming a blanket dielectric layer having a third thickness on the second layer and within the recess and on top of the first layer within the recess, said blanket dielectric layer being on the sidewalls of the second layer, the third thickness being half or less that of the second thickness;

selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers on the sidewalls of the second layer and to remove the blanket dielectric layer from a bottom of the recess;

etching the first layer to expose the substrates and form a gap having a width equal to the selected dimension between the dielectric spacers;

forming a fourth layer in the gap and on the substrate; and

removing any remaining portions of the second layer without removing the dielectric spacers.

44. The method of claim 43 wherein forming a first layer comprises forming two chemically distinct sub-layers on the surface of the substrate, each being selectively etchable with respect to the other, the combined sub-layers comprising the first layer having the first thickness.

45. The method of claim 43 wherein forming a first layer comprises:

forming a thermal oxide on the substrate, the substrate formed from silicon;

forming a silicon nitride layer having a thickness of less than five hundred Angstroms on the thermal oxide.

46. The method according to claim 43 wherein said second layer is formed of silicon dioxide having a thickness of approximately five thousand Angstroms.

47. The method according to claim 43 wherein said step of removing any portions remaining of the second layer is performed prior to forming a fourth layer in the gap. --

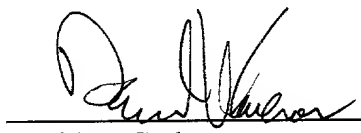
REMARKS

With this continuation application, claims 14-20 of the original application are presented for examination, together with new claims 43-47. These claims are directed towards a method of forming a feature having a selected dimension and are believed patentable in light of all prior art of record. In particular, the method steps carried out by Chau et al. are distinctly different from the method steps as claimed in the present invention. The claimed features are not taught in, or obvious in light of Chau et al. Or other prior art of record. Accordingly, allowance of all claims is respectfully requested.

Respectfully submitted,

Robert Louis Hodges

Seed Intellectual Property Law Group PLLC



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